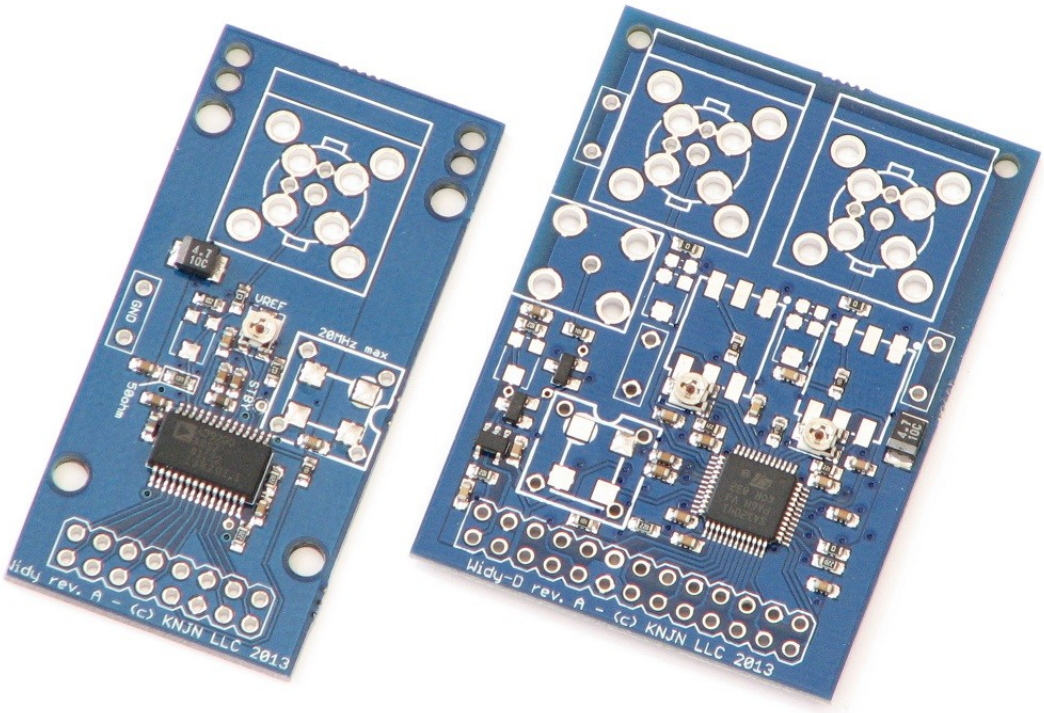
Widy acquisition board

http://www.knjn.com/

Widy rev. A
Widy-D rev. A, B, C



Document last revision on **May 26, 2015**

Table of Contents

1 Introduction

1.1 What are Widy and Widy-D?

They are an analog-to-digital converter (ADC) board, commonly used with an FPGA board.

1.2 Widy

- Single input converted to 10bit @ 20Msps (based on Analog Devices AD9200).
- DC-coupled, adjustable impedance input (50Ω default).
- Full range adjustable from 0.0V..+1.0V to 0.0V..+2.0V
- Input connector BNC or SMA.
- Clocked using an on-board oscillator, or from an outside source.
- Powered using 3.3V and consumes about 20mA

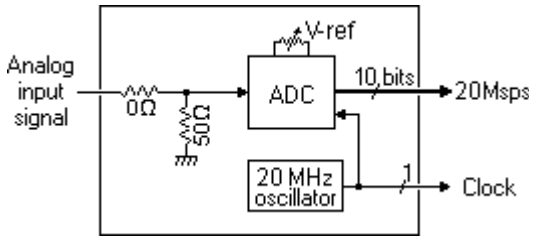
1.3 Widy-D

- Dual inputs converted to 12bit @ 20Msps (based on STMicroelectronics TSA1204).
- DC-coupled, adjustable impedance input.
- Full range adjustable from -0.4V..+1.4V to -0.1V..+1.7V
- Input connector BNC or SMA.
- Clocked using an on-board oscillator, or from an outside source.
- Powered using 3.3V and consumes about 50mA

2 How they work

2.1 Widy

Here's Widy block diagram.

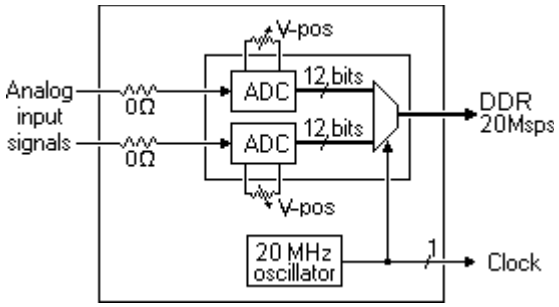


The input on the left is analog, while the outputs on the right are digital.

- The analog input signal is fed to the ADC (AD9200) which digitizes the signal and creates a 10bit 20Msps output.
- The ADC is clocked from a 20MHz local oscillator. The 20MHz clock signal is also made available outside Widy, so that the 10bit output can be synchronously captured. Optionally, the oscillator can be disabled or removed to allow the clock to be fed from an external source.
- The V-ref potentiometer allows adjusting the ADC input range between 0.0V..+1.0V to 0.0V..+2.0V
- The 0Ω pass-through input resistor can be changed to increase the input voltage range. For example, changing it to 450Ω creates a 10:1 input stage and allows voltages up to 20V to be sampled.

2.2 Widy-D

Here's Widy-D block diagram.



The inputs on the left are analog, while the outputs on the right are digital.

- The analog input signals are fed to the ADC (TSA1204) which digitizes the signal and creates a DDR 12bit 20Msps output.
- The ADCs are clocked from a 20MHz local oscillator. The 20MHz clock signal is also made available outside Widy-D, so that the DDR 12bit output can be synchronously captured. Optionally, the oscillator can be disabled or removed to allow the clock to be fed from an external source.
- The V-pos potentiometers allow adjusting the ADCs input position between -0.4V..+1.4V to -0.1V..+1.7V
- The input range can be increased by changing the input resistors.

3 ADC output header

3.1 Header

Widy/Widy-D use standard 0.1” (2.54mm) pitch headers and are compatible with all KNJN FPGA boards.
All signals are high-speed logic signals and may require terminations.

3.2 Widy pinout

Widy uses a 2x8 header.

DA0 (pin 2)	GND	DA3	DA5	GND	VCC (3.3V)	DA8	GND (pin 16)
DA1 (pin 1)	DA2	DA4	DA6	Clock	VCC (3.3V)	DA7	DA9

3.3 Widy-D pinout

Widy-D uses a 2x13 header.

(pin 2)	GND		D11	GND	VCC (3.3V)	D9	GND (pin 16)	D7	D5	D3	GND	D1 (pin 26)
(pin 1)				Clock	VCC (3.3V)	D10	D8	D6	GND	D4	D2	D0